In the Claims:

Please amend claim 5-7, and add new claims 8-17 as indicated below. This listing of claims replaces all prior versions.

1. (Previously presented) A method of powering an integrated circuit, said integrated circuit comprising a chip within a package assembly, said chip comprising a plurality of logic circuits, each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, the method comprising the steps of:

measuring the power voltage supplied to the integrated circuit, and

regulating this power voltage in order to keep the difference between the measured voltage and a reference voltage as small as possible,

wherein during the measuring step the power voltage is directly measured within the chip at the power input of at least one of the logic circuits, and

wherein the method comprises the step of setting the reference voltage such that the voltage supplied to the power input of at least one logic circuit of the chip is equal to the predetermined maximum operating voltage of this logic circuit.

2. (Previously presented) The method according to claim 1, wherein during the measuring step the power voltage is measured within the chip directly at the power input of the logic circuit known to be the first to be damaged in the case of a power voltage increase on at least one power input lead of the integrated circuit.

3. (Previously presented) The method according to claim 2, wherein during the measuring the power voltage is measured within the chip directly at the power input of the logic circuit known to be supplied with the highest power voltage available within the chip.

4. (Previously presented) The method according to claim 1, wherein, during the measuring step the power voltage is measured within the chip directly at the

power input of a first logic circuit, and wherein during the setting step, the reference voltage is set to the value of the predetermined maximum operating voltage of a second logic circuit known to be the first to be damaged in the case of a power voltage increase on at least one power input lead of the integrated circuit minus a margin voltage representative of a voltage drop between the power inputs of the first and second logic circuits.

5. (Currently amended) A powering system comprising:

an integrated circuit comprising a chip within a package assembly, said chip comprising a plurality of logic circuits, each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, and the package comprising at least one power input lead,

a power supply to supply a power voltage to said at least one power input lead, said power supply being able to regulate the power voltage supplied in dependence on the difference between a reference voltage and a voltage measured at a sensing point,

wherein the sensing point is ~~placed~~ located within the chip of the integrated circuit at the power input of one of the logic circuits, and

wherein the reference voltage is set so as to supply to the power input of at least one logic circuit a voltage equal to the predetermined maximum operating voltage of this logic circuit.

6. (Currently amended) The system according to claim 5, wherein the sensing point is ~~placed~~ located at the power input of the logic circuit known to be the first to be damaged in the case of a power voltage increase on said at least one power input lead.

7. (Currently amended) An integrated circuit ~~comprising~~ comprising,

a chip within a package assembly, said chip comprising a plurality of logic circuits, each of the logic circuits having at least one power input which should

not receive a power voltage exceeding a predetermined maximum operating voltage, the package assembly being provided with a plurality of leads to be connected to an external circuit board, one of these leads being a sensing lead to measure the voltage directly at a sensing point within the chip and another lead being a power input lead, wherein the sensing point is ~~placed~~ located at the power input of the logic circuit known to be the first to be damaged in the case of a power voltage increase on the power input lead.

8. (New) The system according to claim 5, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having an impedance, and wherein the sensing point is located at the power input of the logic circuit that is connected to the power input pad by the track having the lowest impedance.

9. (New) The system according to claim 5, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having a length, and wherein the sensing point is located at the power input of the logic circuit that is connected to the power input pad by the track having the shortest length.

10. (New) The system according to claim 5, further comprising a comparator that determines the difference between the reference voltage and the voltage measured at the sensing point, the comparator located external to the integrated circuit.

11. (New) The system according to claim 5, wherein the sensing point is located at the power input of the logic circuit known to be supplied with the highest power voltage available within the chip.

12. (New) The method according to claim 1, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having an impedance, and

wherein the power voltage is measured at the power input of the logic circuit that is connected to the power input pad by the track having the lowest impedance.

13. (New) The method according to claim 1, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having a length, and wherein the power voltage is measured at the power input of the logic circuit that is connected to the power input pad by the track having the shortest length.

14. (New) The method according to claim 4, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having an impedance, and wherein the power input of the second logic circuit is connected to the power input pad by the track having the lowest impedance.

15. (New) The method according to claim 4, wherein the chip includes a power input pad and the power input of each of the logic circuits is connected to the power input pad by a respective track, each track having a length, and wherein the power input of the second logic circuit is connected to the power input pad by the track having the shortest length.

16. (New) The method according to claim 4, further comprising determining the difference between the reference voltage and the measured voltage using a comparator that is located external to the integrated circuit.

17. (New) The method according to claim 4, wherein the power input of the second logic circuit is supplied with the highest power voltage available within the chip.